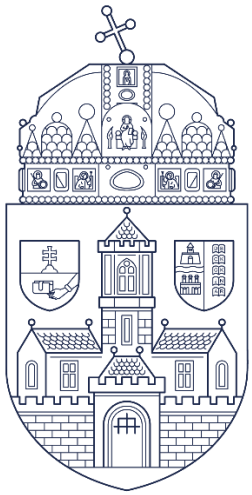
Óbuda University

PhD Thesis Summary



High Performance Image Signal Processing using Field Programmable Gate Arrays

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1 Background

1.1 FPGAs

During the past 40 years Field Programmable Gate Arrays (FPGAs) were first transformed from a uniform sea-of-gates architecture [1] to a heterogenous multiprocessing System-on-a-Chip (SoC) platform. With relentless miniaturization and specialization, modern devices have the capacity and features to implement complex machine vision algorithms [2],[3].

In the first phase of this transition, 18kbit memories (Block RAMs) were added to the devices, followed by 18bit multipliers, and specialized clocking resources. Simple multipliers were expanded to 48-bit Digital Signal Processing (DSP) blocks. The devices were split to tiles, some having specialized functions. With Virtex2-Pro, hardened processors integrated into the Programmable Logic (PL) fabric were offered for the first time [3].

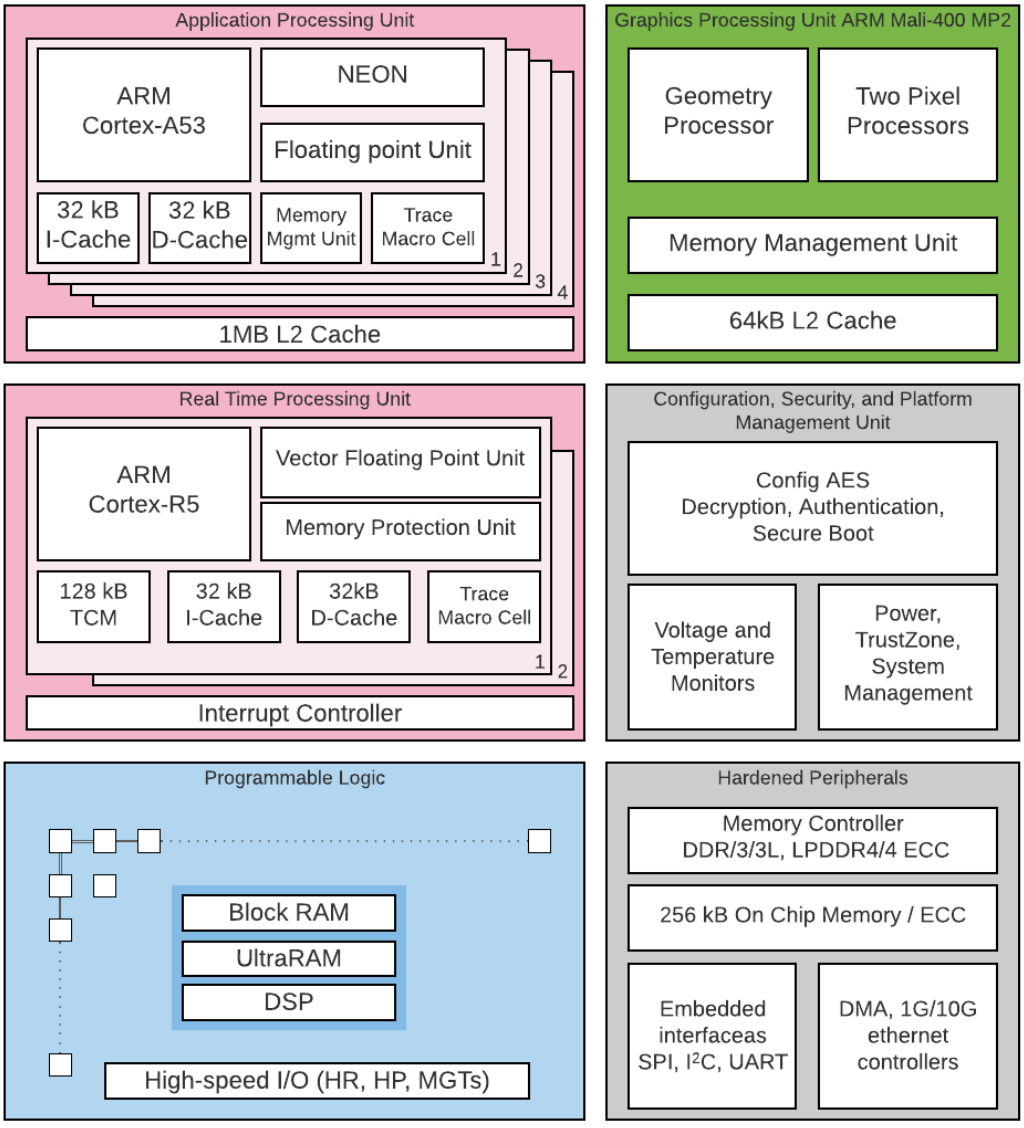

Figure 1: Example block diagram of a modern FPGA device, the Xilinx Zynq Ultrascale+ MPSoC[1]

[1] Source: adapted from https://www.xilinx.com/products/silicon-devices/soc/zynq-ultrascale-mpsoc.html

The latest generation of FPGA devices include multicore, heterogenous processing system (PS, the pink block on Figure 1), GPUs (Green area), and various hardened functions, such as Memory and Network controllers, peripherals, such as I2C, SPI controllers, DMA and watchdog timers. Thousands of DSP engines with single precision floating point units with integrated hierarchical cache memories can implement complex, high performance video processing solutions. Beyond implementing SIMD or MIMD architectures, fine grain configurability enables FPGAs to implement custom DSP and image processing blocks, allowing multiple trade-offs between area, performance, and numerical precision.

1.2 Image Signal Processing

Multi-core, general purpose processors may outperform FPGAs for complex image processing operations. However, for custom, high frame rate camera systems FPGAs remain the best design choice. FPGAs are ideal for implementing demanding image and signal processing algorithms due to the inherent parallelism of logic resources.
Recognition, registration, and reconstruction all need consistent, high-quality images [4]. The purpose of Image Signal Processing (ISP) is to condition images for higher level image and video processing functions. As opposed to other machine vision platforms, such as GPGPU SoCs, like the Nvidia Xavier AGX [5], specialized ASICs, like the Intel Movidius Myriad [6], or mobile platforms, like the Qualcomm 865 [7], FPGAs do not currently have hardened ISP units. While other embedded system processors have dedicated, proprietary ISP pipelines, FPGAs offer PL resources, tightly integrated with a system processor (PS).

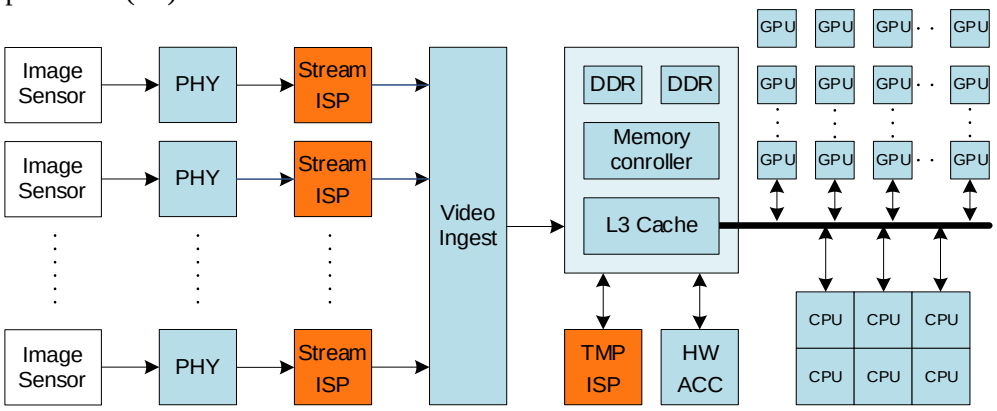

Figure 2: Example implementation of a machine vision platform

Figure 2 presents a typical machine vision platform, with multiple image sensors providing input to processing algorithms executed on an array of GPU and CPU cores. Image sensors typically connect to the platform via MIPI CSI2.0 DPHY or CPHY, sLVDS, or parallel CMOS interfaces. FPGAs provide high-speed I/O features to receive, de-serialize, and deinterleave streams (PHY block on Figure 2).

The spatial ISP functions can be performed directly on the image streams, without having access to previous frames. The Streaming ISP pipeline block can perform:

- Flat-field and pixel defect correction,
- Lens shading, and (limited) distortion correction,
- Bayer Color Filter Array (CFA) interpolation,
- Spatial edge enhancement and noise removal,
- Color correction,
- Tone mapping,
- Video format conversion (chroma resampling, video scaling)

The received frames are subsequently stored in video frame buffers, and are made available to a second set of ISP functions, performing functions, such as:

- Motion adaptive temporal noise reduction,
- Image composition and affine transformation e.g., rotation and/or translation
- Temporal resampling, e.g., frame rate changes or High-dynamic-range (HDR) processing

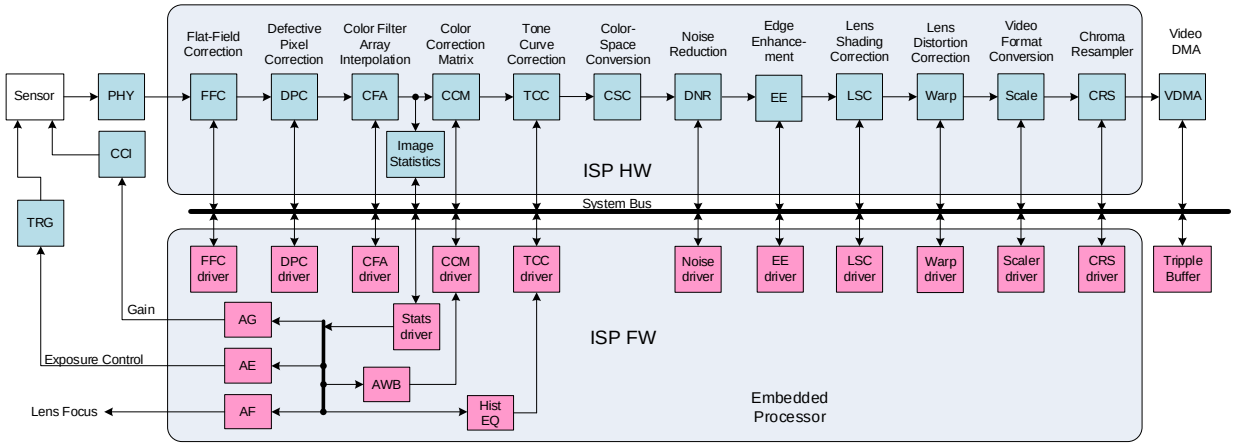

Figure 3: Streaming ISP pipeline HW and FW components

Figure 3 illustrates a typical streaming ISP pipeline, with blue functional units implemented in FPGA PL as custom accelerators, with corresponding drivers and low-level ISP functions (pink blocks) implemented as firmware executed in the FPGA PS.

1.3 Sensor Control

Besides conditioning image streams, ISPs initialize image sensors and adjust processing parameters, such as exposure time, to maintain optimal imaging conditions. Automatic Exposure Control (AE), Automatic White Balancing (AWB), and Automatic Focus (AF) adjustment, often referred to as "3A" [8] are functions the ISP need to perform with minimal latency after image acquisition. Namely, after each exposure, while the frame is being read out from the sensor, image statistics need to be gathered and evaluated. Based on the statistical data, the 3A processing engine needs to set new exposure parameters and control the voice coils of the lens assembly to maintain focus. Similar to the effects of latency introduced to a fed-back control loop, if frames were first committed to a frame buffer, then read back out and analyzed for statistics, the latency introduced would create a system difficult to control.

Image sensors typically contain programmable gain amplifiers, which can scale analog voltages read out from pixel capacitors, before analog to digital conversion (ADC). At low signal levels, a higher gain value may lift the signal out of quantization noise, however, higher gain also amplifies thermal and electric noise in the system. Based on priority (exposure or gain) settings of the camera, the AE algorithm controls exposure time and analog gain (AG) on a frame-by-frame basis. Gain values are programmed via the Camera Control Interface (CCI), which is typically an I2C or SPI register interface. Exposure times may be programmed via the register interface as well, but for stereo cameras performing visual odometry, where precise timing of exposure periods require synchronization of exposure pulse centers, dedicated logic (TRG) is necessary to generate exposure trigger pulses.

1.4 Flat-Field Correction

Flat-field Correction (FFC) aims to remove fixed-pattern image artifacts introduced by non-uniformity of the sensor or the optical system. Some machine vision applications, such as visual odometry and single-pixel airborne object tracking, are extremely sensitive to pixel-to-pixel sensitivity variations. FFC allows the correction of:

- Dark Signal Non-Uniformity (DSNU), pixel-to-pixel differences in dark current,
- Photo Response Non-Uniformity (PRNU), pixel to pixel sensitivity differences,
- vignetting, or lens shading,
- other optical defects, such as light scratches or contamination.

For correcting the DSNU, a set of reference images are collected with no exposure – often with the sensor covered [9]. To correct PRNU, a large set of reference images with uniform illumination are captured, and combined into a single frame, referred as the flat frame [10].
Due to the characteristic, row/column separable nature of DSNU and PRNU, for high-resolution cameras high-frequency pixel to pixel correction is often performed by row and column projections of calibration images [11]. In this case, lens-shading correction is performed by a separate ISP module based on parametric vignetting model of the sensor-lens system. For low resolution cameras where local RAM resources can store a compressed, or uncompressed calibration frame, full pixel to pixel compensation for low and high-frequency defects can be applied. The flat-field corrected image can be given formally as:

$$I_{FFC} = \frac{I - I_D}{I_F - I_D} m - c,, \tag{1}$$

where I is the input image to be corrected, I_D is the dark calibration image, I_F is the flat calibration image, and m and c are constants to adjust the output brightness and black level, respectively.

1.5 Defective Pixel Correction

An image sensor may have defects affecting individual pixels, or clusters. Affected pixels may have significantly altered dark currents (hot pixels), sensitivities (dead pixels), or excessive noise load (flickers) [12]. Sensors failing image quality checks are discarded by manufacturers. Most defects affecting machine vision systems arise during use by high energy particles impacting photodiodes. The purpose of defective pixel correction (DPC) is the identification and interpolation of defective pixels. In static solutions, locations of defects outside the range correctable by FFC are identified during FFC calibration and are stored in a Look-Up-Table. During regular operation sensor images are not analyzed for defective pixels, but defective pixel locations are interpolated on the fly.
Dynamic solutions analyze the sensor data stream and look for outlier pixels, which are apparently stuck or flicker independent of neighboring pixel values and local motion. While dynamic solutions are significantly more complex and often require access to frame buffers, they can keep up with the degradation of the sensor due to the detection of accumulating pixel defects.

1.6 Noise Reduction

1.6.1 Gaussian Noise Removal

Sources of imaging noise in order of significance are: shot-, electronic-, and thermal-noise are de-correlated and can be modelled as additive Gaussian noise[22]. Several effective methods have been adopted widely to denoise images and video streams:

- Spatial filtering techniques, such as bilateral filtering [13],
- Temporal (motion compensated, or motion adaptive) IIR filtering [14],
- Machine learning based methods [15],

While novel FPGAs can implement any of these approaches, for streaming ISPs without access to an external frame buffer, pure spatial filters are the most efficient option.

1.6.2 Rank Order Filtering

Rank order filtering is a non-linear filtering technique, which selects an element from an ordered list of n samples. Median filters, for example, are examples of rank order filters where the element in the middle of the ordered list, with index $\lfloor n/2 \rfloor$, is selected. Compared to linear filters, such as FIR or IIR, rank filters can effectively remove impulse-like noises while preserving high frequency content of the original stream. For image and video processing, rank order filters can be extended to two-dimensional (2D) filters, which remove "salt-and-pepper" noise while preserving the edges of the original image. This can be useful for removing transmission (bit-flip) artifacts, especially as pre-processing for edge detection.
2D filtering takes place on the contents of a rectangular window, which slides across the image. Every time the h pixel high by w pixel wide window is moved by one pixel, h obsolete pixels are discarded, and h new pixels are inserted to the kernel. The filter has to sort hw pixels to generate an output pixel. Due to predominance of comparison operators and subsequent branch misprediction median filtering is not efficiently carried out by GP processors or ALUs.

1.7 Color Processing and Image Enhancements

Color image sensors use a CFA overlay to enable differential spectral sensitivity between adjacent photodiodes in the sensor array. The Bayer CFA is the most commonly used arrangement of color mosaic filters [20], using Red, Green, and Blue (RGB) or Cyan, Magenta and Yellow (CMY) dyes. The mosaic pattern is laid out in repeating RGRG…RG, and GBGBG..GB lines (Figure 4).

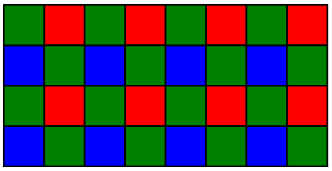

Figure 4. Example of the Bayer RGB Color Filter Array pattern

From one measured color component per pixel, the ISP needs to re-create all 3 color components by interpolating the two missing components using data from neighboring pixels. A critical input to the interpolation process is the phase alignment of the CFA: whether the top line of the image frame contains red or blue pixels, and if the top left pixel is green or not. If CFA interpolation is performed with incorrect assumptions on the color filter positions, the resulting images can be useless due to extreme color artifacts.

The measured color and intensity of light from a small, uniform surface element with no inherent light emission or opacity depend on three functions: the spectral power distribution of the illuminant, the spectral reflective properties of the surface material, the spectral sensitivities of the imager.
The trichromatic aggregate spectral power measured by image sensor pixels inherently mix the native color of objects with the spectral content of the illuminator. White balance estimation is based on heuristics about color content of the scene. Subsequent color correction aims to restore colors that appear correct regardless the illuminant (daylight, incandescent, fluorescent).

Enhancement of features, such as edges and contours, is a typical image pre-processing operation, improving not only the visual appearance of captured images but the accuracy and performance of downstream recognition and classification tasks [16]. Simple approaches like Canny and Sobel edge detectors produce predictable results, but are sensitive to noise, distort texture and unlikely to connect broken edges. Robust algorithms often rely on context from image pyramids or persistence of features across multiple image frames. However, these pre-processing features are seldom available for the streaming ISPs. The enhancement of features in the presence of noisy input continues to remain an area of active research.

1.8 Custom Image Processing Accelerators

Many image processing tasks, such classification, recognition, tracking, stabilization, and optical flow calculation depend on two dimensional searches in image regions. An extensible set of complex instructions, such as two-dimensional correlation or convolution, can be effectively accelerated by performing the search in the frequency domain [16]. In order to facilitate performing these operations on FPGAs, efficient implementation of Fast forward-, and inverse Fourier transforms was an active research area.

1.8.1 Fourier Transform modules

The Fast Fourier transform (FFT) is a computationally efficient algorithm for computing a discrete Fourier transform (DFT), defined as

$$X[k] = \sum_{n=0}^{N-1} x[n] W_N^{kn} \ , \ x[n] = \frac{1}{N} \sum_{k=0}^{N-1} X[k] W_N^{-kn} \ , \tag{2}$$

1.8.2 Phase Factor generation for DFT and FFT

Silicon area in HW implementation of FFTs with more than 2048 points are dominated by memory [39]. Processing Elements (PE) in pipelined FFT processors have designated phase factor generators to provide periodic harmonic sequences. In a loop-engine structure, the single processing node needs all possible twiddle-factor combinations, W_N^{nk} (k>1, $0 \le n$<N/r). Twiddle factors are accessed in a fixed order, meaning the phase increment is constant. This allows recursive calculation of samples, which can lead to significant savings in logic complexity.

1.8.3 Direct Digital Synthesis

The Direct Digital Synthesis (DDS) block introduced by Tierney et.al. [18] consists of a phase accumulator and a phase to sinusoid converter, and generates samples of a harmonic function with frequency

$$f = f_{ref} \frac{\Delta\phi}{2^M}, \tag{3}$$

where $\Delta\varphi$ is the phase increment or frequency control word, M is the width of the phase accumulator and f_{ref} is the frequency of the reference clock. The original DDS does not lend itself well for high point-size, high precision FFTs, as memory size grows exponentially by the width of φ and linearly by the width of the output. Consequently, for low-noise and high period length DDS applications, where an exclusively memory-based solution would be prohibitively large, an under-sampled memory is used with refinement circuitry to interpolate between samples stored in memory.
The quality of the generated harmonic stream can be assessed by computing the Spurious Free Dynamic Range (SFDR),

$$SFDR = 20 \log \frac{A_{signal}}{A_{\max\_spur}}, \tag{4}$$

where A_{signal} is the amplitude of the signal, the strongest spectral component, and $A_{\max\_spur}$ is the amplitude the worst spur, which is the second strongest spectral component.

2 Research Goals

High framerate, high resolution video acquisition-, and pre-processing are areas at the crossroads of high-speed I/O interfaces, and custom, high-speed signal processing. The primary goal of my research was to study, improve, and adapt Image Signal Processing algorithms to FPGAs. Since the beginning of this work in 1996, FPGA platforms, the complexity of image processing algorithms, and performance expectations developed exponentially.
A secondary goal of the research activity was to reduce the barrier of entry using FPGAs as practical machine vision platforms. Back then, and still today, developers and researchers needed an Image Signal Processing pipeline to effectively convey images from an image sensor of their choice to the machine vision hardware accelerator of their design. Imaging SoC developers often keep details of their proprietary ISP subsystems and 3A algorithms trade secrets. To bridge this gap, compact, efficient modules have to be designed, implemented, documented and distributed. My continued research is focused on perfecting and publishing AE, AWB and denoising algorithms using the embedded HW components detailed in the thesis. My goal for AE and AWB was to provide methods which were at par or better than the performance of benchmark platforms at the time, in terms of stability, accuracy and convergence time.

In case of Flat-Field correction, the dependence of DSNU and PRNU of state-of-the-art CMOS image sensors over temperature and sensor gain was analyzed and modeled, to find a compact correction solution that lends itself well for ASIC or FPGA implementation.

For image de-noising median-, and rank-order filters were evaluated for FPGA implementation. While optimization of sorting algorithms was well understood at the time, efficient mapping of one-dimensional median filters to FPGAs were an area of research. We aimed to find a solution to generalize an architecture to 2D rectangular, and non-rectangular filter kernels, which could process streaming video, namely in a single cycle ingest multiple pixels and produce an output pixel.

To accelerate one-, and two-dimensional correlations and convolutions, often carried out in the frequency domain FFTs and IFFTs had to be mapped efficiently to FPGA PL resources. Specifically, scarce local memory resources had to be conserved. My goal on this field was to optimize memory accesses and data movements within parts to ensure compact, efficient architectures. I have evaluated scientific literature looking for alternatives to twiddle factor storage, such as variants of the CORDIC algorithm [19] and DDS [23][24], and pursued improvements to reduce the footprint of twiddle synthesis circuitry. My goal was to design a twiddle-factor generator which is optimal in the following terms:

- generate sin/cos with $N \geq 2^{16}$ samples period length
- SFDR >150 dB
- minimal slice, memory and multiplier count.
- compute both quadrature components simultaneously.
- support twiddle-factor access in reverse order, to support IFFT calculations.

3 Methods of Investigation

Each functional module of the ISP pipeline was thoroughly researched before the candidate implementation most suited for FGPA implementation was selected. Prior art from published conference and journal publications was analyzed for performance and applicability. An excellent example of this is Bayer CFA interpolation, for which numerous algorithmic approaches [20] were implemented using high level languages (Matlab or C++) to evaluate performance. Algorithmic improvements and simplifications were proposed and their effects on algorithmic complexity and image quality were evaluated using the Kodak Image Dataset [21]. The full precision reference model of the most promising prospective algorithm was selected for arithmetic optimization.

A set of optimization techniques were deployed to reduce the complexity of arithmetic operations. Quantization noise along arithmetic pipeline was evaluated to find the optimum resolution of operands while translating floating point to fixed-point operations. Performance of the fixed-point, bit-accurate reference model was evaluated against the full-precision model to quantify noise and image artifacts introduced.

The optimized, fixed-point architecture was implemented in either Verilog, or VHDL hardware Description Languages. Functional verification of the HDL model was performed using logic simulation. A Verilog, or SystemVerilog test-bench was developed, to consume stimuli and golden result files generated by the bit-accurate reference model, and to verify numerical performance. Code and functional coverage targets were established wherever necessary.

Xilinx (now AMD), Altera (now Intel), and Lattice FPGAs were used for the physical implementation of designs. Synthesis reports were used to compare resource usage of the improved ISP modules, and timing reports were consumed to verify operating performance.

To enhance ease-of-use and adaption, Graphical User Interfaces (GUI) were created for the modules. Performance metrics were collected and compiled into a comprehensive datasheet describing parameterization options, typical use scenarios and results.

4 New Scientific Results

Thesis group I: Contributions to ISP Image Quality improvements

Statement 1.1: *I performed in-depth analysis of temperature and analog gain dependence of fixed pattern noise of modern CMOS image sensors. I proposed FFC and ISP architectures, optimized for FPGA or ASIC implementation supporting different noise suppression performance and resource trades.*

Image Sensor nonuniformity and lens system characteristics were known to be temperature dependent. Numerous cameras, especially on the fields of infrared imaging and staring cameras, use multiple calibration images to correct for nonuniformities. My research characterizes the temperature and analog gain dependence of DSNU and PRNU of two contemporary global shutter CMOS image sensors for machine vision applications.

An optimized hardware architecture was proposed to compensate for nonuniformities, with optional parametric lens-shading correction. For both DSNU and PRNU, compensation with one or multiple calibration images, captured at different gain and temperature settings, as well as compensation with interpolated calibration images were evaluated. Based on model results, the effectiveness, external memory bandwidth, power consumption, implementation-, and calibration complexity of different nonuniformity correction approaches were compared.

Own publications pertinent to this statement: [25], [53], [26]

Statement 1.2: *I provided an algorithm and architecture for automatic detection of single-pixel and cluster defects on focal-plane array images, optimized for FPGA implementation.*

In comparison with existing methods, the proposed architecture requires no external frame-buffer access, therefore lends itself well for FPGA and VLSI implementation of streaming ISPs. In contrast with state-of-the-art algorithms, the proposed solution can effectively identify slowly varying temporarily defective pixels. With excellent convergence speed and accuracy, it also supports monochrome-, or color (Bayer CFA) sensors.

Own publications pertinent to this statement: [26], [48]

Thesis group II: Contributions to Color Correction of Image Sensor Streams

Statement 2: *I provided a method for color calibration, an algorithm suitable for low-power embedded processors and its efficient implementation on FPGAs for robust white balancing of image streams.*

The proposed algorithm leverages a hardware accelerator ISP module, implemented in FPGA logic fabric, which calculates focused, luminance weighted 2D Chrominance histograms. Illuminant estimation is performed by real-time classification of 2D chrominance histograms of image frames, comparing against illumination specific signature patterns established offline. Classifier output probabilities are filtered using temporal, adaptive IIR filters, which in turn control the mixing of color-calibration matrixes specific to illuminants. Besides efficient use of FPGA resources and low embedded processor load, one advantage of the proposed method is that correction errors due to illuminant misclassifications are bound, preventing gross distortion of image colors.

Own publications pertinent to this statement: [25], [47], [52], [52]

Thesis group III: Efficient Implementation of Rank Order Filters

Statement 3.1: *I demonstrated that FPGAs are ideal implementation platforms for 1D median filters, and I proposed an architecture that resulted in a compact, high-performance solution.*

The complexity of the ordering operation is strongly affected by the size of the kernel size *N*, with complexity scaling with $\theta(N\log(N))$. General purpose DSP processors exhibit sharply decreasing performance with increasing *N* due to inefficient pipelining and prediction misses caused by data dependent jumps in sorting algorithms. The proposed FPGA implementation can implement real-time median or rank order filters for high-speed video processing applications efficiently with dedicated ISP HW that scales with *N*, processing each input sample in a single clock cycle. Existing bit-serial approaches provide compact, low-footprint solutions, but does not support high dynamic range imaging. Word parallel sorting networks tend to use logic resources inefficiently. The proposed insert-delete architecture stores samples ordered by magnitude, resulting in compact footprint, and high performance even for high-dynamic range images.

Own publications pertinent to this statement: [31], [32], [33], [34]

Statement 3.2: *I proposed an efficient, generalized structure for 2D rank order filtering, capable of processing a configurable number of pixels in a single clock cycle.*

A word serial architecture is presented first, which stores samples in the order they were received. The novel architecture is extended to word-parallel processing multiple input samples per clock cycle, enabling efficient implementation of 2D rank order filters. A solution is presented to optimize the filter by balancing performance (filter clock frequency vs. video clock frequency) and parallelism (number of pixels processed per clock cycle). Use cases of the proposed filter for color image processing, and non-rectangular kernels are presented.

Own publications pertinent to this statement: [28], [29], [30], [40], [49]

Thesis group IV: Efficient Implementation of Fast Fourier Transforms

Statement 4.1: *I proposed methods and architectures to reduce the depth of memory buffers by 50% for in-place FFT implementations by eliminating double buffering.*

2D FFT and IFFT operations are important preprocessing steps for image classification. Local memories for sample and twiddle factor storage are critical resources to be optimized for FPGA FFT implementations. I have shown that with a large number of parallel multipliers and adjacent local memories, FPGAs can implement FFT/IFFT operations with configurable transform lengths efficiently, providing trade-offs between resource allocation and transform time. As point sizes (*N*) increase, HW implementations with $N > 4096$ are dominated by memory allocation. In previous implementations data frames were double buffered for in-place / loop-engine configurations to facilitate random access to samples without output samples overwriting input samples.

Own publications pertinent to this statement: [36], [37], [38], [59]

Statement 4.2: *I proposed a method to reorganize input data to an FFT from natural to digit-reversed order, or results of an FFT from digit-reversed order to natural order without double-buffering frames.*

Decimation In Time (DIT) processing structures expect the input data frame in bit/digit reversed order and generate an output frame in natural order. A Decimation In Frequency (DIF) FFT expects the input frame in natural order, but the output frame is in bit/digit reversed order. To access input and output samples in natural order, a reorganizer stage is necessary, which in previous implementations double-buffered the frame.

Own publications pertinent to this statement: [50], [58]

Statement 4.3: *I proposed a novel Direct Digital Synthesis architecture for sine / cosine synthesis optimized for twiddle-factor generation (W_N^{nk}) for FFTs, using a quadratic differentiator – integrator structure. I proposed a cascaded architecture using a digital resonator as the primary, and a continuous quadratic interpolating secondary stage as a high-quality, compact twiddle-factor source for large ($N>2^{17}$) FFTs.*

Twiddle factors (W_N^{nk}) for FFT computations are traditionally pre-computed and stored in a single LUT with coarse-rotation logic. For 36 bit coefficients, sufficient for most applications, this solution maps efficiently to FPGA BRAMs for $N \leq 2^{11}$. For $N > 2^{11}$, however, BRAM counts grow proportional to N. Targeting these applications, I adapted two existing twiddle factor generation QDDFS architectures for FFTs for optimal implementation in FPGAs. The quadratic differentiator-integrator based QDDFS can supply coefficients with SFDR>410 dB for $2^{12} \leq N \leq 2^{16}$, using only one BRAM. With configurable subsampling- and interpolation length, as well as configurable phase addressing of the BRAM based LUT, the solution can provide twiddle factors for in-place processing engines, dynamically configuring ranks for $N \leq 2^{16}$ FFTs. For larger point-sizes, a bit-serial digital resonator solution can replace the BRAM based LUT to provide samples to be interpolated by the quadratic interpolator stage. The resonator computes 63-bit complex twiddle factors in 128 CLK cycles. The solution demonstrated superior compression ratios and very low noise compared to other methods available, using slice-based logic only allocating less than 550 registers. The cascaded architecture demonstrated SFDR>370 dB and SNR>160 dB for $N \geq 2^{17}$ points. For comparable numerical performance, the CORDIC algorithm requires more than 2000 registers. The direct (LUT) + coarse rotation implementation for this performance level would require 72 BRAMs.

Own publications pertinent to this statement: [39], [56]

5 Practical Applicability of the Results

After an initial period of theoretical exploration of FPGA architectures, practical 2D FFT implementation on Altera Flex10k FPGAs developed in academia were performed for DARPA/ITO under contract DABT63-97-C-0020, at the time to be considered for US defense purposes [36][37].

A significant portion of the ISP module research activity was performed while employed by Xilinx Inc, now part of AMD. Working with inbound marketing on customer interest in FPGA modules to assist with image sensor interfaces, research had to be focused on market driven activities directly tied to specific lead customers. The result of these activities: the Color Correction Matrix[2], CFA interpolation[3], Chroma Re-sampler[4], Video Scaler[5], Tone Mapping[6], and Image Enhancement[7] modules have been assisting Xilinx customers, engineers, and researchers with free, high quality image processing blocks for FPGA image sensor interface implementations.

Optimized DSP modules, such as the complex multiplier [35] and the high speed FFTs were showcased as Technology demonstrators for Virtex devices and continue to exist in Xilinx Beamformer applications.

Reference designs and application notes, such as [8]XAPP953 for the Two-dimensional Rank Order Filter, or the RGB to YCrCb[9] and YCrCb to RGB[10] color space converters helped FPGA users to adopt using the ISP block-set.

My research directly contributed the 1080p60 Camera ISP design to development kits, such the Zynq Video and Imaging Kit[11], released in 2013, also announced by EE Times[12].

While commercial research and development is less conducive to open publication of results at public conferences and journals, during the 12 years at Xilinx I published 15 US patents [45]-[59].

Since 2014 my research contributed to avionics video product development. FPGA design modules were contributed to a multichannel, high-definition, high framerate, mixed mode, custom designed video interface card. The FPGA and corresponding PCB product has been part of ION[13], an avionics video-, audio-, and data recorder currently sold by Shotover Systems.

US Patent 10674063 [44] is a contribution to the synchronization of Time-of-Flight (ToF) cameras currently employed in Amazon Go stores[14].

My work on the field of Auto-Exposure, and Flat-Field correction of CMOS sensors was performed for Amazon Prime Air. The resulting video processing modules and corresponding firmware is being used in second generation delivery vehicles[15]

[2] https://www.xilinx.com/products/intellectual-property/ef-di-ccm.html
[3] https://www.xilinx.com/products/intellectual-property/v_demosaic.html
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